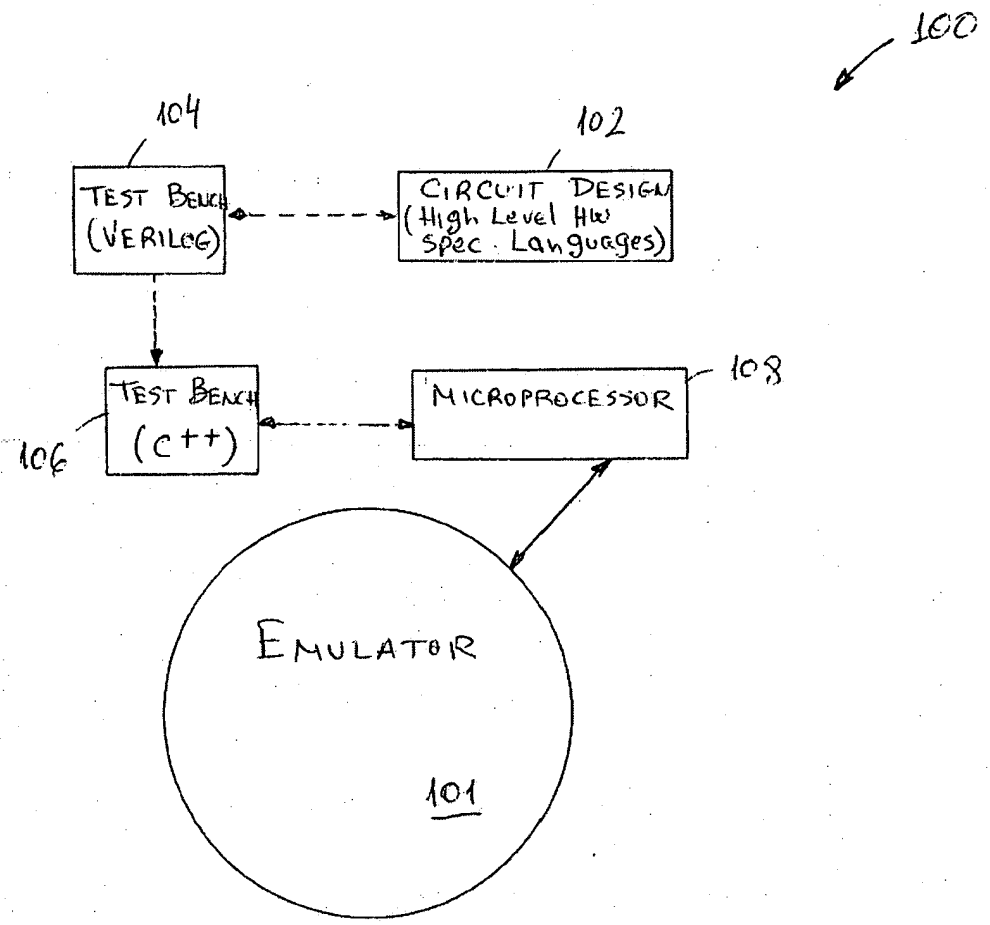

FIGURE 1

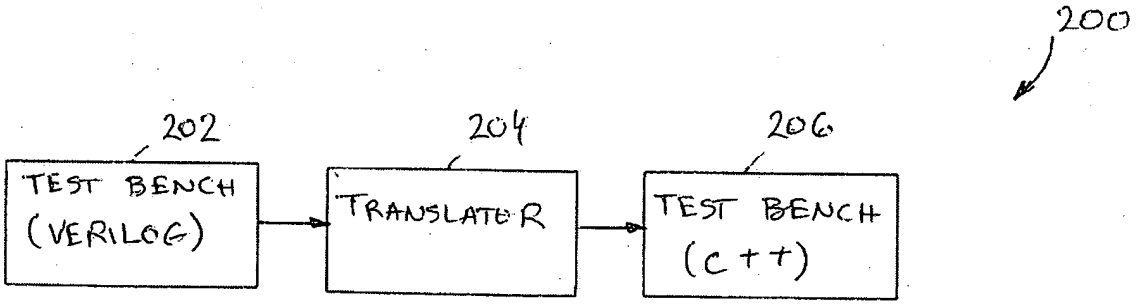

FIGURE 2

VERILOG PATTERN	C++ PATTERN / ACTION
# delay statements	Remove # delay statements
`idef statements	Translate `idef statements
` symbols	Remove ` symbols
Begin	{
End	}
Register definitions	Convert register definitions
Combinatorial assignments	Convert combinatorial assignments
Events	Convert events
Verilog switches	Convert Verilog switches
Verilog Concat expressions	Convert Verilog Concat expressions
Verilog parameters	Convert to C ++ #defines
Verilog consts	Convert to C consts
Verilog bit access macro	Convert bit access macro

FIGURE 3

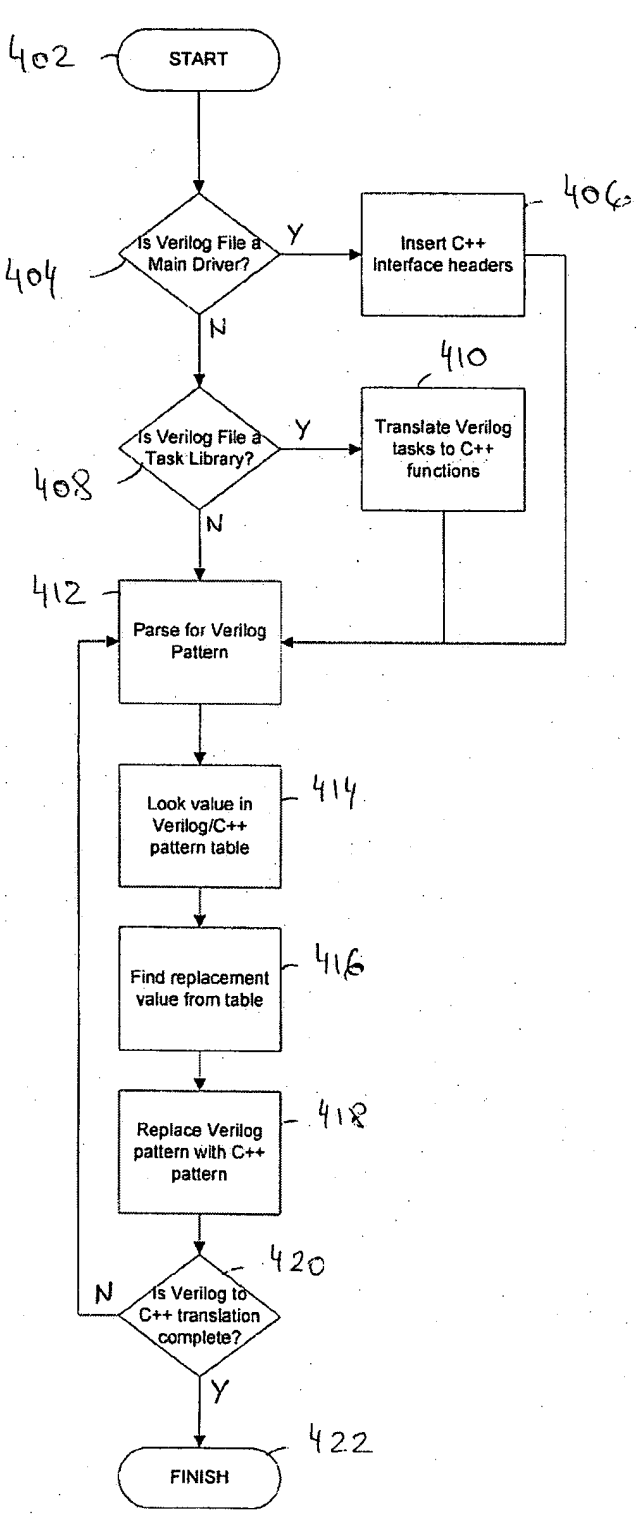
400
402
START
404
Is Verilog File a Main Driver?
Y
406
Insert C++ interface headers
N
408
Is Verilog File a Task Library?
Y
410
Translate Verilog tasks to C++ functions
N
412
Parse for Verilog Pattern
414
Look value in Verilog/C++ pattern table
416
Find replacement value from table
418
Replace Verilog pattern with C++ pattern
420
Is Verilog to C++ translation complete?
N
Y
422
FINISH

FIGURE 4

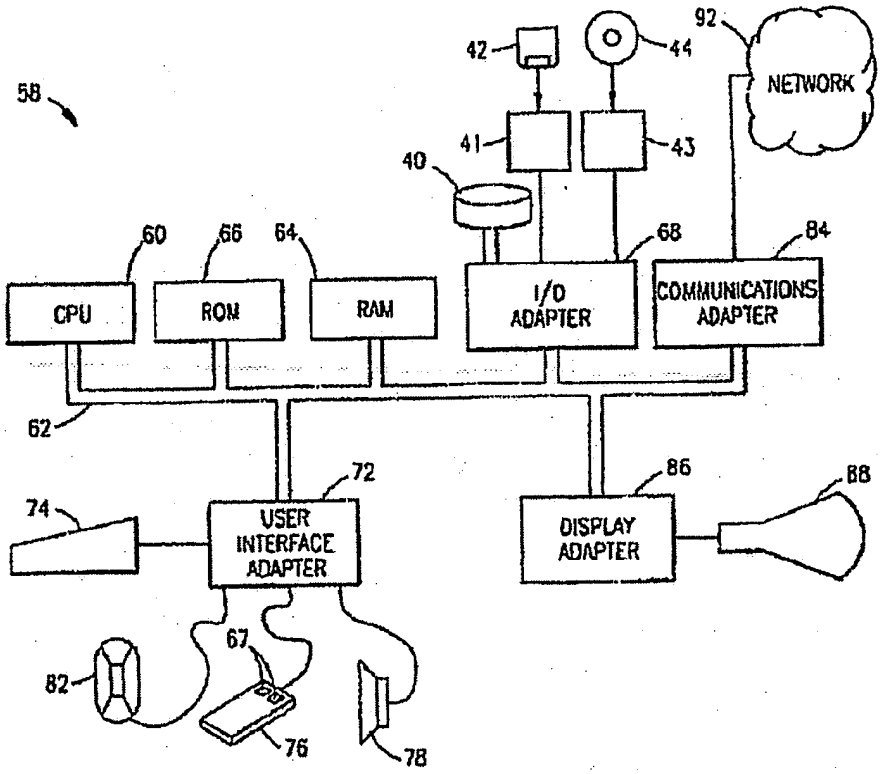
58
42
44
92
NETWORK
41
43
40
60
66
64
68
84
CPU
ROM
RAM
I/O ADAPTER
COMMUNICATIONS ADAPTER
62
72
74
USER INTERFACE ADAPTER
86
88
DISPLAY ADAPTER
67
82
76
78

FIGURE 5